IN THE SPECIFICATION

Please replace paragraph on page 3, starting on line 17:

Figure 2 is a flow chart illustrating a method to recover data [[to]] according to an aspect of the present invention;

Please replace paragraph on page 5, starting on line 1:

Sender system 110 encodes a sequence of data tokens in an analog signal, and transmits the [[an]] analog signal over serial communication channel 119. Sender system 110 encodes data tokens using a clock signal of a specified frequency (e.g., 622 MHz, 1.28 GHZ, etc). In an embodiment described below, each token represents a bit having one of two possible values.

Please replace paragraph on page 7, starting on line 11:

Clock recovery circuit 310 generates bits by sampling analog signal 391 (DIN) at time points specified by an internally generated sampling clock (not shown), and the generated bits are provided on line 315. It may be noted that the data (on 315) recovered directly according to the sampling clock by clock recovery circuit 310 is ignored (but the desired data is recovered) in the described embodiment. The ignored data could be erroneous, particularly in the presence of a high amount of

jitter in input clock signal [[111]] 119.

Please replace paragraph on page 10, starting on line 11:

In addition, DOUT_FINAL 155 may need to be aligned with the falling edge of CLKOUT_FINAL signal on line 159. To achieve the alignment, CLKOUT signal 319 is provided to delay block 380 to generate CLKOUT_FINAL on line [[389]] 159. The amount of delay may equal the propagation delay of flip flop 370 and multiplexor 340. The rising edge of CLKOUT_FINAL 389 occurs in the center of DOUT_FINAL on line 159.